REMARKS

Upon entry of the Amendment, claims 1-10 and 16 will be all the claims pending in the application. Claims 11-15 have been canceled without prejudice by this Amendment. New claims 17 and 18 find support, for example, bridging pages 11-12 of the specification.

Applicants affirm the election without traverse of claims 1-10 and 16, and reserve the right to file a divisional application directed to the non-elected subject matter.

No new matter has been added. Entry of the Amendment is respectfully requested.

I. Claim Rejections under 35 U.S.C. § 103

Claims 1-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US 20030133256; "Yoshida"), in view of Yoshimura (US 4,864,472), and in further view of Kamigawa et al. (US 6,139,592; "Kamigawa").

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US 20030133256), in view of Yoshimura (US 4,864,472), and in further view of Kamigawa et al. (US 6,139,592) and Fawcett et al. (US 4,192,721).

Claims 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US 20030133256), in view of Yoshimura (US 4,864,472), and in further view of Kamigawa et al. (US 6,139,592).

Applicants respectfully traverse the above rejections.

None of the cited references, either alone or in combination, discloses or suggests the jig for producing capacitors, as recited in independent claims 1 and 2.

Independent claims 1 and 2 both recite a jig for producing capacitors, which is used for forming a semiconductor layer by means of energization on two or more electric conductors each having formed on the surface thereof a dielectric layer, wherein the jig comprises two or more

current ejection-type constant current sources each having an output electrically connected in series with a connection terminal for the electric conductor.

Yoshida was relied upon as teaching a jig for producing capacitors, which is used for forming a semiconductor layer 3 by means of energization on two or more electric conductors 10 each having formed on the surface thereof a dielectric layer 2.

The Examiner acknowledged that Yoshida fails to explicitly show the jig comprising two or more current ejection-type constant current sources. The Examiner asserted that Yoshida teaches a power supply as the source, each having an output electrically connected in series with a connection terminal for the electric conductor 10. Figures 8 and 2-7, Paragraphs 37-41.

Yoshimura was relied upon as teaching (Figure 1, column 4, lines 60-61) use of a constant current source 5 and forming polymerization layer (organic semiconductor) 14 on the dielectric 13 coated anode 12 (3). The Examiner asserted that it would have been obvious to incorporate the above features of Yoshimura in Yoshida because the constant source/diode would limit the current to a predetermined constant value for the deposition process.

The Examiner further acknowledged that the combination of Yoshimura and Yoshida yet fails to disclose the instantly claimed invention. Specifically, the combination of Yoshimura and Yoshida fails to disclose or teach two or more current ejection-type constant current sources, as recited in independent claims 1-2.

Kamigawa was then relied upon to make up the deficiency of Yoshida and Yoshimura.

The Examiner asserted that Kamigawa teaches (figure 5, column 6, lines 41-43) two or more current ejection-type constant current sources (diodes 50 and 51) each having an output electrically connected in series with a connection terminal for the electric conductor 31/211.

The Examiner considered that it would have been obvious to incorporate the above features of Kamigawa in the combination of Yoshimura and Yoshida for the benefit reducing leakage current. Applicants respectfully disagree.

In particular, Fig. 5 of Kamigawa relied upon by the Examiner has nothing to do with forming a semiconductor layer. Rather, Fig. 5 is an apparatus for aging a plurality of capacitor elements by applying a dc voltage thereto in an environment of the highest temperature around which the capacitor is to be used. A current limiter 51 is arranged for each of the capacitor elements one individually, presumably to block excess current in case one of the capacitor elements becomes short-circuited.

Applicants respectfully submit that there is insufficient motivation to combine the cited references.

Specifically, because Kamigawa is not concerned with forming a semiconductor layer, and because Kamigawa employs current limiter 51 so as to restrict current flow, there is no apparent reason which would lead one of ordinary skill to apply the configuration of Kamigawa to the apparatus of Yoshimura (where there is no concern for limiting current flow). Yoshimura shows constant current source 5, but this is not a current ejection-type constant current source (such as a diode), and as noted by the Examiner, there is no teaching or suggestion to apply a constant current source in series with each connection terminal.

In this connection, the instant specification discloses at pages 2-3, that in the case of forming a semiconductor layer by means of energization on an electric conductor having formed thereon a dielectric layer as described above, no problem arises when a semiconductor layer is formed on one electric conductor, but when two or more electric conductors are processed, individual electric conductors are not necessarily homogenous or the semiconductor formation

rate may vary among electric conductors. In particular, when a semiconductor layer is formed simultaneously on multiple electric conductors, variation in the current value of the electrical current flowing through the electric conductors gives rise to production of capacitors uneven in the formation of semiconductor layer in some cases, *and this makes it difficult to produce capacitors stabilized in the capacitance.* As a result of intensive investigations to solve these problems, the present inventors have found that *when the semiconductor layer is formed by supplying a constant current to electric conductors, capacitors having a small variation in the capacitance can be obtained.* None of the cited reference recognizes or discloses this aspect of the claimed invention.

In addition, Kamigawa relates to an aging treatment of the capacitor element for an organic solid electrolyte capacitor. In Kamigawa, all of a dielectric layer, a semiconductor layer, a carbon layer and a silver paste layer have been formed on the anode body before the aging treatment. In such an aging treatment, a positive electrode of a power supply is electrically connected to the anode body of the capacitor element, while the silver paste layer of the capacitor element is electrically connected to the negative electrode of a power supply via a current limiter.

Kamigawa employs a current limiter is used to block excess current in case one of the capacitor elements becomes short-circuited in the dielectric layer. That is, the current limiter is not working if a short-circuit does not arise.

To the contrary, the present invention relates to the formation of a semiconductor layer and a treatment performed before a carbon layer and a silver paste layer are formed, different from the aging treatment of Kamigawa.

Also, there is a gap between the conductor (anode body) and the negative electrode of the jig for producing capacitors in the present invention and no direct electrical connection between them. Accordingly, the present invention does not need the function of a current limiter in order to prevent short-circuiting since the short-circuiting problem solved by Kamigawa when subjecting completed capacitors to aging treatment is not encountered when forming a dielectric layer.

A diode (constant current source) in the present invention applies a predetermined electric current to each of the plural conductors (anode bodies). That is, all of the diodes function at the time of forming semiconductors, while the current limiter of Kamigawa does not work unless a problem arises.

As discussed above, although diodes (constant current sources) are used in the current limiter of Kamigawa, the purpose of use and function thereof is totally different from those of the present invention and also not applicable to Yoshida which also relates to forming a semiconductor layer. Therefore, Applicants believe that Kamigawa cannot reasonably be combined with the other cited references.

In view of the above, Applicants respectfully request reconsideration and withdrawal of the foregoing §103 rejections. Withdrawal of all rejections and allowance of claims 1-10 and 16 is earnestly solicited.

II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Yan Lan
Registration No. 50,214

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